1. A method of recording test information to identify a location of errors in integrated circuits (ICs) comprising:

scanning a plurality of ICs with an input signal, each IC having a plurality of data locations;

comparing an output response at each data location with an expected value for the data location; and

storing addresses in a buffer for each data location at which the response at the data location does not equal the expected value corresponding to the data location.

2. The method of claim 1, further comprising sending a data string to a storage device containing the addresses.

3. The method of claim 2, wherein sending the data string includes:

sending a header containing an x-address, a y-address, and a scan-address;

sending a series of device addresses; and

sending a trailer.

4. The method of claim 3 wherein sending a series of device addresses includes sending an extension.

5. The method of claim 2, wherein sending the data string includes:

sending a header containing an x-address, a device address, and a scan address;

sending a series of y-addresses; and

sending a counter having a count of y-addresses.

6. The method of claim 1, wherein sending the addresses includes sending a memory address and a location of the IC.

7. The method of claim 1, further comprising placing the ICs on a burn-in board.

8. The method of claim 1, further comprising leaving the ICs on a wafer.

9. The method of claim 1, further comprising using memory cells as the data locations.

10. The method of claim 1, further comprising limiting a number of comparisons between the output response and the expected value to a specified number.

11. The method of claim 1, further comprising filtering out ICs having failed a front-end test.

12. A system of recording test information to identify a location of an error for integrated circuits (ICs) comprising:

at least one comparator comparing an output response at each of a plurality of data locations in a plurality of ICs with an expected value corresponding to the data locations; and

a processor scanning the at least one comparator at each data location and the processor sending addresses to a buffer when the response at each data location does not equal the expected value.

13. The system of claim 12, further comprising a data storage device that receives the addresses in a data string.

14. The system of claim 13, wherein the data string includes:

a header containing an x-address, a y-address, and a scan-address;

a series of device addresses; and

a trailer.

15. The system of claim 14 wherein each device address includes an extension.

16. The system of claim 13, wherein the data string includes:

a header containing an x-address, a device address, and a scan address;

a series of y-addresses; and

a counter having a count of y-addresses.

17. The system of claim 12, wherein the addresses include a memory address and a location of the IC.

18. The system of claim 12, wherein the ICs are on a burn-in board.

19. The system of claim 12, wherein the ICs are on a wafer.

20. The system of claim 12, wherein the data locations are memory cells.

21. The system of claim 12, further comprising a data stack for must repair compression.

22. The system of claim 12, further comprising a fail mask logic.